**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

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| In re application of: | Fye | Group Art Unit: | 2421 |
| Serial No.: | 10/699,311 | Examiner: | Smith |
| Filed: | October 30, 2003 | Confirmation No.: | 3928 |
| For: | AN ARCHITECTURE FOR MULTI-CHANNEL VIDEO | | |
| Docket No.: | H0005246 (002.2154) | | |
| Customer No: | 89955 | | |

# APPEAL BRIEF PURSUANT TO 37 C.F.R. §41.37

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant hereby submits its Appeal Brief in response to the final rejection of the subject patent application.

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## Introduction

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the rejections set forth in the final Office Action dated March 09, 2010. Each of the topics required by 37 C.F.R. §41.37 is presented in this Appeal Brief and is labeled appropriately.

## II. Real Party In Interest

Honeywell International, Inc. ("Honeywell") is the real party in interest of the present application. An assignment of all rights in the present application to Honeywell was executes by the inventors and recorded by the U.S. Patent and Trademark Office at Reel 014673, Frame 0570.

## III. Related Appeals and Interferences

There are no appeals or interferences related to the present application of which Appellant is aware.

## IV. Status of the Claims

Claims 1-28 are pending in the application. Claim 29 has been cancelled without prejudice or disclaimer. Each of claims 1-28 stand finally rejected. Accordingly, the Appellant hereby appeals the final rejection of claims 1-28.

## V. Status of Amendments

There have been no claim amendments filed subsequent to the final rejection.

## VI. Summary of Claimed Subject Matter

The instant application presents subject matter that relates to an apparatus 102 for display of video data from a plurality of video sources 115A-N (Page 8, lines 3-13). Independent claim 1 recites a plurality of video channels 116A-N configured to be coupled to different video sources 115A-N and a plurality of video decoders 206A-N coupled to the plurality of video channels116A-N, each video decoder 206A-N coupled to a different one of the plurality of video channels 116A-N (Page 9, lines 3-15). The video decoders 206A-N comprise an output and an input (FIG. 2) coupled to one or more video channels 116A-N to receive video data from the one or more video channels, and to decode the received video data (FIGs. 2 and 4-408; Page 9, lines 16-27). The apparatus 102 includes a switch network 208 including an output and an input coupled to the video decoder outputs and a plurality of video processing pipelines 212A-P, each video processing pipeline 212A-P including an input coupled to the switch network output, wherein the switch network 208 is configured to connect any of the video decoder outputs to any of the video processing pipeline inputs (FIG. 2; 3A-3C; Page 10, lines 1-10). The apparatus 102 also includes a manual I/O interface 110 in operable communication with the plurality of video processing pipelines 212A-P, the manual I/O interface110 configured to provide an option to a user to direct the switch network 208 to connect a specific video decoder output to a particular view window of the apparatus for display (Page 10, lines 15-27).

Independent claim 7 recites a method 400/500 for displaying video data from a plurality of video sources 115A-N on a display 112 (Pages 16-19). The method comprises receiving video data 402 from each of the plurality of video sources 115A-N via a plurality of video channels 116A-N and decoding 408, with a plurality of video decoders 206A-N, at least a portion of the video data received from the plurality of video channels 116A-N, each video decoder 206A-N receiving video data via a different video channel (Page 9, lines 9-17). The method further comprises inputting 414 the decoded portion of the video data into a plurality of video processing pipelines 212A-P via a switch network 208 (Page 10, lines 1-10) and processing, by the plurality of video processing pipelines, the decoded portion of the video data (Page 10-11-14). The method further comprises providing a user an option to select one of the video channels

116A-N decoded by a specific video decoder 206A-N for viewing in a particular view window of the display 112 via a manual I/O interface 150/152 that is in operable communication with the plurality of video processing pipelines 212A-N (Page 10, lines 14-20).

Independent claim 14 recites a method 400//500 for displaying video data from a plurality of video sources 115A-N via a plurality of video channels 116A-N in a display device 112. The method comprises receiving first video data from a first video source 115A-N at a first video decoder 206A-N via a first video channel 116A-N and receiving second video data from a second video source 115A-N at a second video decoder 206A-N via a second video channel 116A-N (Page 9, lines 3-15). A first frame of the first video data and a second frame of the second video data are then decoded via the first video decoder 206A-N and the second video decoder 206A-N (Page 9, lines 16-20; Page 13, lines 20-27). The method also comprises inputting the first decoded frame into a first video processing pipeline 212A-N via a non-blocking switch network 208 and inputting the second decoded frame into a second video processing pipeline 212A-N via the non-blocking switch network 208 (Page 10, lines 1-8; Page 14, lines 3-10). The method proceeds by processing the first decoded frame and the second decoded frame by the first video processing pipeline 212A-N and the second video processing pipeline 212A-N, respectively (Page 11, line 25-Page 12, line 3). The method also comprises transmitting the processed first decoded frame into a first portion of a video buffer 228A for updating the display device 112 with the processed first decoded frame, storing the second processed decoded frame into a second portion of the video buffer 228B that is not updating the display device112 (Page 12, lines 19-26; Page 16, lines 1-5), and providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device 112 via a manual I/O interface 150/152 that is in operable communication with the first and second video processing pipelines 212A-P (Page 16, lines 23-26).

Independent claim 19 recites a system 100 for displaying video data on a display device 112. The system comprises a plurality of video sources 115 A-N, a plurality of video channels 116 A-N coupled to the plurality of video sources 115A-N (Page 8, lines 9-12), wherein each of the plurality of video sources 115A-N is configured to transmit

first video data to a different one of the plurality of video channels 116A-N (page 8, lines 6-7; FIG. 1). The system 100 also comprises a video logic 102 coupled to the plurality of video channels 115A-N (Fig. 2). The video logic 102 comprises a plurality of video decoders 206A-N. Each of the plurality of video decoders 206A-N is configured to receive the first video data from a different one of the plurality of video sources 115A-N and to decode the first video data (FIG. 2; Page 9, lines 3-15). The video logic 102 further comprises a plurality of video processing pipelines 212A-N, and a switch network 208 coupled to the plurality of video decoders 206A-N and the plurality of video processing pipelines 212A-N (FIG. 2) (page 10, lines 1-10), the switch network 208 being configured to connect any of the plurality of video decoders 206 A-N to any of the plurality of video processing pipelines 212A-N (Page 10, lines 1-10), wherein one of the plurality of video processing pipelines 212A-N is configured to process the decoded first video data from a portion of the plurality of video decoders 206A-N (Page 14-16). The system 100 also comprises a manual I/O interface 110 in operable communication with the plurality of video processing pipelines 212A-N, the manual I/O interface 110 being configured to provide an option to a user to direct the switch network 208 to display the first video data in a particular view window of the display device 112 (Page 16, lines 23-26).

## VII. Grounds of Rejection to be Reviewed On Appeal

Whether the combination of the European Patent 1,158,788 ("Machida") in view of U.S. Patent Publication 2002/0147987 ("Reynolds") and further in view of U.S. Patent Publication 2002/0078447 ("Mizutome") renders claims 1, 4-5, 7-8, 11-12, 19 and 22 obvious under 35 U.S.C. §103(a).

Whether the combination of Machida, Reynolds, Mizutome, in view of U.S. Patent 6,118, 498 ("Reitmeier"), and further in view of U.S. Patent 5,883,676 ("Miyazaki") renders claim 14 obvious under 35 U.S.C. §103(a).

Whether the combination of Machida in view of Reynolds, Mizutome and U.S. Patent 6,456,335 ("Miura") renders claims 23-25 obvious under 35 U.S.C. § 103(a).

Whether the combination of Machida in view of Reynolds, Mizutome and U.S. Patent Publication 2002/0150248 ("Kovacevic") renders claim 26 obvious under 35 U.S.C. § 103(a).

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## VII. Argument

Applicant respectfully submits that claims 1-28 are allowable over the various combinations of the current set of asserted references. Applicant also submits that claims 14, 23 and 25-26 stand on their own and do not stand or fall with independent claims 1, 7 and 19 or with each other.

### A. The combination of *Machida, Reynolds* and *Mizutome* does not render independent claims 1, 7 and 19 obvious under 35 U.S.C. §103(a).

Independent claim 1 recites, inter alia:

"[a]n apparatus for display of video data from a plurality of video sources, the apparatus comprising…a plurality of video decoders coupled to the plurality of video channels, each video decoder coupled to a different one of the plurality of video channels…"

To render a claim obvious, the cited references must disclose each and every element of the rejected claim as interpreted in light of the Applicant's specification (see MPEP §2143).

In her rejection of independent claim 1, the Examiner asserts that *Machida* describes most of the claim elements but concedes that *Machida* fails to describe "a plurality of video decoders coupled to the plurality of video channels, **each video decoder coupled to a different one of the plurality of video channels**." The Examiner then proceeds in her rejection by asserting that *Reynolds* cures this discrepancy in *Machida* and in doing so expressly equates the various decoders in FIG. 2 (220, 224, 228) of *Reynolds* to the recited video decoders and equates the video signals 102, 128 and 108 of *Reynolds* to the recited "channels" in support of her rejection.

However, Applicant respectfully submits that *Reynolds* fails to describe the subject matter ascribed to it by the Examiner when interpreted in light of the Applicant's specification. For example, *Reynolds* fails to describe that "each video decoder [is] coupled to **a different one** of the plurality of video channels."

*Reynolds* expressly describes that a single multiple video feed 206 is provided to a tuner/decoder 208. The tuner/decoder 208 somehow extracts the different component

signals (210,212) from the multi-video feed 206 that carries the video signals (102, 104, 108) (Para. [0041]).

*Reynolds* continues on to describe that the video signal 210 is applied to a video decoder 220 to decode the signal and store the decoded signal into RAM 222. Then, in turn, video decoder 224 receives an interactive video feed 212 and stores the decoded signal into RAM 226. Finally, video decoder 228 is operated in similar fashion with RAM 230 (Paragraph [0044]). Hence, *Reynolds* describes that the tuner/decoder 208 receives the multiple feed (110, 206), extracts a particular video signal 210 and sends it to the decoder 220 which processes it and records it temporarily in RAM 222. The tuner/decoder 208 then repeats the process with interactive video feed 212. Thus, only one decoder (220, 224, 228) is coupled to one video signal (102, 128, 108) at a time by tuner/decoder 208. Hence, *Reynolds* does NOT describe "a plurality of video decoders coupled to the plurality of video channels, **each [i.e., all] video decoder [is] coupled to a different one of the plurality of video channels.**" Rather the tuner/decoder 208 in *Reynolds* only couples one decoder to a video signal at a time, and by logical extension decouples the others. Thus, **each** (i.e., all) video decoders (220, 224, 228) cannot be coupled to a **different one** of a plurality of video channels incoming from the multi-channel feed 206.

Because Reynolds fails to describe that each video decoder is coupled to a different one of the plurality of video channels, *Reynolds* fails to cure the conceded deficiencies in *Machida*. Therefore, the combination of *Machida* and *Reynolds* fails to establish a prima facie case of obviousness in regard to independent claim 1 because the alleged combination fails to describe each and every claim element.

In her Advisory Action mailed May 11, 2010[1], the Examiner attempts to rebut Applicant's argument by redefining the term "channel" by pointing out that the IEEE definition of the term "channel" is a "**signal path** for transmitting electric signals, usually in distinction from other parallel paths." She then asserts that, based on this definition, *Reynolds* then describes "a plurality of video decoders are coupled to the plurality of video channels [i.e. signal paths], each video decoder coupled to a different one of the plurality of video channels [i.e. signal paths]."

[1] And for the first time during prosecution.

Applicant respectfully submits that the Examiner's asserted definition of "channel" is improper and respectfully points out that the claims must be given their broadest reasonable interpretation, but this interpretation must be **consistent with the specification** (MPEP 2111) and that an Applicant may be his own lexicographer (MPEP 2111.01). In this respect, Applicant respectfully points to paragraph [0003] of the specification where it is expressly disclosed that "[a] typical synchronized 'n' channel analog video rendering system (**displaying 'n' video channels simultaneously**) displays the video at…**the National Television Standards Committee (NTSC) analog video format standard.**" (emphasis added). Throughout the specification, it is a video or **television channel** that is being discussed under the NTSC standard and not a physical signal path for transmitting signals under the particular IEEE standard asserted by the Examiner. Thus, the Applicant's express definition of "channel" is a television channel (i.e. an electronic signal) under the NTSC standard must prevail.

Further, assuming for the benefit of this argument only that the Examiner's definition of "channel" as a physical signal path is proper, Applicant respectfully points out that the tuner/decoder 208 of *Reynolds* prevents a plurality of physical signal paths (102, 104 and 108) from being coupled to decoders 210, 212, 214 because it only couples one decoder at a time to one signal path. As such, *Reynolds* fails to describe a plurality of video decoders are coupled to the plurality of signal paths, each video decoder coupled to a different one of the plurality of signal paths as well.

In regard to *Mizutome*, *Mizutome* describes a single video decoder 106 coupled to multiple video channels via a tuner 101 that selects a single channel. This description is also contrary to a plurality of video decoders coupled to a plurality of video channels, each video decoder coupled to a different one of the plurality of video channels. Therefore, *Mizutome* fails to cure the above discussed deficiencies in the combination of *Machida* and *Reynolds*.

For any of the above reasons, a prima facie case of obviousness cannot be established because none of *Machida, Reynolds*, *Mizutome* or their combination describe "a plurality of video decoders coupled to the plurality of video channels, each video decoder coupled to a different one of the plurality of video channels." As such, independent claim 1 is allowable over the combination of *Machida, Reynolds* and

*Mizutome* for at least this reason. Independent claims 7 and 19 recite similar subject matter and are allowable for at least the same reasons. Claims 2-6, 8-13 and 20-28 properly depend from an allowable independent claim 1, 7 or 19 and are allowable therewith.

B. The combination of *Machida, Reynolds, Mizutome, Miyazaki* and *Reitmeier* does not render independent claim 14 obvious under 35 U.S.C. §103(a).

Independent claim 14 recites, in pertinent part:

"[a] method for displaying video data from a plurality of video sources via a plurality of video channels in a display device, comprising…inputting the first decoded frame into a first video processing pipeline via a non-blocking switch network;
inputting the second decoded frame into a second video processing pipeline via the non-blocking switch network…"

To render a claim obvious, the cited references must disclose each and every element of the rejected claim (see MPEP § 2143). Applicant respectfully submits that the combination of *Machida* in view of *Reynolds*, *Reitmeier*, *Miyazaki* and *Mizutome* fails to describe inputting decoded frames into a video processing pipeline via a **non-blocking switch.**

In her final rejection, the Examiner **concedes** that *Machida* fails to describe inputting the first and second decoded frames into a first and second video processing pipeline via **a non-blocking switch** (OA page 13, lines 14-17). The Examiner then asserts that *Reynolds* describes "inputting the first decoded frame" and "inputting the second decoded frame" but while doing so **implicitly concedes** that *Reynolds* also fails to describe a non-blocking switch by omitting any assertion to the contrary (OA page 14, lines 14-17).

Applicant respectfully points out that *Reynolds* actually fails to teach a non-blocking switch between the video decoder (220, 224) and a processing pipeline (224,226,232,238). In fact, *Reynolds* fails to describe any switch at all between the output of video decoders (220,224,228) and the rest of the processing pipeline (224, 226, 232, 238). Because a non-blocking switch is not described by *Reynolds*, *Reynolds* fails to cure the conceded deficiency in *Machida*.

Further, Applicant respectfully submits that none of *Reitmeier*, *Miyazaki* and *Mizutome* describes a "non-blocking switch" or inputting the first decoded frame into a first video processing pipeline via a **non-blocking switch** network" or "inputting the second decoded frame into a second video processing pipeline via the **non-blocking switch** network…"

Because none of *Reitmeier*, *Miyazaki* or *Mizutome* describe a non-blocking switch and, therefore, cannot cure the conceded discrepancies in the combination of *Machida* and *Reynolds*, a prima facie case of obviousness cannot be established because the combination of *Reitmeier*, *Machida*, *Reitmeier*, *Miyazaki* and *Mizutome* fails to describe each and every claim element. As such, independent claim 14 is not rendered obvious by the combination of *Reitmeier*, *Machida*, *Reitmeier*, *Miyazaki* and *Mizutome* for at least this reason.

Further, a prima facie case of obviousness cannot be established due to a lack of motivation to combine *Machida* with any of the other references because *Machida* teaches away from the claim elements (MPEP 2145 (X)(D)). This is so because *Machida* teaches away from the use of a non-blocking switch (See, paragraph 0033 (image selection means 101 selects and outputs a prescribed number of images among the input images having high priority orders)). Passing along images in order of priority is antithetical to a non-blocking switch because each image cannot be processed/displayed concurrently without hindrance.

*Machida* expressly describes that images may only enter a processing channel 102 based on their priority assignment, which by definition entails a blocking mechanism and is contrary to a non-blocking switch. Therefore, there is no motivation to combine *Machida* with any of *Reynolds*, *Reitmeier*, *Reitmeier*, *Miyazaki* and *Mizutome* with a reasonable chance of success because *Machida* teaches the use of a blocking switch arrangement that relies on image priority as discussed above. As such, independent claim 14 is allowable over the current combination of references for at least this additional and independent reason. Claims 15-18 properly depend from independent claim 14 and are allowable therewith.

In her Advisory Action mailed May 11, 2010, the Examiner attempts to reverse her express concession that *Machida* fails to describe a non-blocking switch. She does

this by merely asserting that somehow the number of images output from the image selection means 101 may reasonably be equal to the number of processing channels 102 without regard for order or dedication to a particular image processing means 106. Applicant respectfully submits that such assertion cannot be substantiated by the text of *Machida* and is merely improper speculation (See, paragraphs [0030-0033] and [0044]).

Further, even assuming that the Examiner's speculation is correct for the sake of this argument only, Applicant respectfully submits that the image selection means 101 of *Machida* is still a blocking switch mechanism regardless of whether or not on some speculative occasions the volume of images input may be equal to the available image processing channel 102. The Examiner's speculation is akin to arguing that that a reference describing a transistor is actually describing a short because on some occasions the transistor is biased to conduct a current. Just because the transistor is biased to conduct current from time to time, it does not follow that the reference is teaching a short circuit and not a transistor. Therefore, even if the Examiner's speculation about *Machida* is correct, the image selection means 101 is still a blocking switch and teaches away from the claim recitations.

C. The combination of *Machida, Reynolds, Mizutome,* and *Miura* does not render independent claim 25 obvious under 35 U.S.C. §103(a).

Dependent claim 25 stands rejected under 35 U.S.C. § 103(a) as being obvious over *Machida* in view of R*eynolds, Mizutome* and *Miura*.

The Examiner rejects claim 25 by asserting that the combination of *Machida* and R*eynolds* describes most of the claim elements but concedes that the combination fails to describe that "the video fail operation comprises an output of a **previous image** for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure." The Examiner proceeds in her rejection by asserting that *Miura* cures the conceded discrepancy and cites Column 20; lines 49-54 and Column 36; lines 20-33 in support.

However, Applicant respectfully points out that *Miura* fails to describe the subject matter ascribed to *Miura* by the Examiner. *Miura* merely describes using a stored bit map such as a logo with an alphanumeric message (See, Col. 20; lines 49-55). A fixed

bit map in memory cannot reasonably be construed to be an output of a previous image for the one of the plurality of video channels because the output of a previous image is ever changing and is determined only by the subject matter being displayed and the timing just prior to the failure. In other words, the previous image is a random image and not a stored static image that is specific to this purpose as is described in *Miura*. Because *Miura* fails to describe "an output of a previous image for the one of the plurality of video channels," a prima facie case of obviousness cannot be established because the combination of *Machida,* R*eynolds* and *Miura* fails to describe each and every claim element. As such, dependent claim 25 is allowable for at least this additional and independent reason.

Further, Applicant also traverses the rejection because claim 25 properly depends from an allowable amended independent claim 19 and is allowable therewith.

D. The combination of *Machida, Reynolds, Mizutome,* and *Kovacevic* does not render independent claim 26 obvious under 35 U.S.C. §103(a).

Claim 26 stand rejected under 35 U.S.C. § 103(a) as being obvious over *Machida* in view of R*eynolds, Mizutome* and *Kovacevic*. The Examiner rejects claim 26 by asserting that the combination of *Machida* and R*eynolds* describes most of the claim elements but concedes that the combination *Machida* and *Reynolds* fails to describe processing "analog video data" (See, final Office Action mailed March 19, 2010, page 19, line 15-16). However, in light of the Examiner's concession, Applicant respectfully asserts that there is no motivation to combine *Kovacevic* with either of *Machida* or R*eynolds* because both *Machida* and *Reynolds* are strictly digital processes and *Kovacevic* is an analog system.

For example, the Examiner has stipulated that the *Reynolds* processes that allegedly reading on the Applicant's base claims all take place in the interactive set top boxes (112, 118), which process strictly digital data. As can be seen form Figure 1 of *Reynolds,* all analog data is converted to digital data prior to being transmitted by **Digital** Video Distribution Network 104. Therefore, no processes occurring in the User's Locations 111 are capable of processing analog data. As such, a prima facie case of

obviousness cannot be established because there is no motivation to modify *Reynolds* (digital processing) by K*ovacevic* (using analog data) because there is no reasonable chance of success (See, MPEP §2143.02) in processing the analog data of *Kovacevic* by the digital circuitry of *Reynolds/Machida*.

Similarly, the Examiner has also stipulated that the *Machida* processes that allegedly read on the Applicant's base claims all occur in the image selection means 100, which processes strictly digital data. As can be seen form FIG. 4 of *Machida,* all video analog data is converted to digital data at A/D converter 213, prior to being transmitted to the digital image selection means 100. Therefore, no processes occurring in the image selection means are capable of processing analog data. As such, a prima facie case of obviousness cannot be established because there is no motivation to modify *Machida* (digital processing) by *Kovacevic* (using analog data) because there is no reasonable chance of success in processing analog data by digital circuitry (See, MPEP §2143.02). For a reasonable chance of success, a primary operating principle of either *Machida* (converting to analog processing) or *Kovacevic* (converting to digital processing), would be required (MPEP §2143.01).

Because there is no motivation to modify either *Machida* or *Reynolds* by the analog data of *Kovacevic,* claim 26 the combination of *Machida, Reynolds* and *Kovacevic* cannot render claim 26 obvious for at least this additional and independent reason.

Further, claim 26 properly depends from an allowable independent claim 19 and is allowable therewith.

## IX. Conclusion of Arguments

In view of the foregoing, Appellant submits that the rejection of claims 1-28 is improper and should not be sustained. Therefore, reversal of the rejections in the Office Action dated March 09, 2010, is respectfully requested.

No fees are believed due beyond the fee for this Appeal. However, please charge any additional fees or credit any overpayment to Deposit Account No. 50-3025.

Respectfully submitted,

July 27, 2010

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## X. Claims Appendix

1. (Previously Presented) An apparatus for display of video data from a plurality of video sources, the apparatus comprising:

a plurality of video channels configured to be coupled to different video sources;

a plurality of video decoders coupled to the plurality of video channels, each video decoder coupled to a different one of the plurality of video channels and comprising:

an output, and

an input coupled to one or more video channels, to receive video data from the one or more video channels, and to decode the received video data;

a switch network including an output and an input coupled to the video decoder outputs;

a plurality of video processing pipelines, each video processing pipeline including an input coupled to the switch network output, wherein the switch network is configured to connect any of the video decoder outputs to any of the video processing pipeline inputs, and

a manual I/O interface in operable communication with the plurality of video processing pipelines, the manual I/O interface configured to provide an option to a user to direct the switch network to connect a specific video decoder output to a particular view window of the apparatus for display.

2. (Previously Presented) The apparatus of claim 1, further comprising an image size/location logic coupled between the manual I/O interface and each video processing pipeline output, the image size/location logic configured to receive a signal indicating a designated size of a display window and which of the plurality of video sources includes

video data for display in the display window, the image size/location logic further configured to determine a location in the display window and a size of a part of the display window for display for the video data for each of the plurality of video sources including video data for display.

3. (Previously Presented) The apparatus of claim 2, further comprising a plurality of scalers coupled to the plurality of video decoders and the plurality of video processing pipelines, wherein the plurality of scalers are each configured to scale the decoded video data from the plurality of video sources based on the determined size of the part of the display window.

4. (Previously Presented) The apparatus of claim 1, wherein the plurality of video processing pipelines are configured to process the decoded video data of the plurality of video sources received from the plurality of video decoders.

5. (Previously Presented) The apparatus of claim 4, wherein the apparatus comprises a greater number of video decoders than video processing pipelines and wherein the apparatus further comprises a display/control logic coupled to the plurality of video processing pipelines, the display/control logic configured to control a process order of the video data from the plurality of video sources.

6. (Previously Presented) The apparatus of claim 1, further comprising:

a memory device; and

a write multiplexer coupled to the memory device and the plurality of video processing pipelines, the write multiplexer configured to receive processed decoded video data from the plurality of video processing pipelines and store the processed decoded video data from the plurality of video sources into the memory device.

7. (Previously Presented) A method for displaying video data from a plurality of video sources on a display, the method comprising:

receiving video data from each of the plurality of video sources via a plurality of video channels;

decoding, with a plurality of video decoders, at least a portion of the video data received from the plurality of video channels, each video decoder receiving video data via a different video channel;

inputting the decoded portion of the video data into a plurality of video processing pipelines via a switch network;

processing, by the plurality of video processing pipelines, the decoded portion of the video data; and

providing a user an option to select one of the video channels decoded by a specific video decoder for viewing in a particular view window of the display via a manual I/O interface that is in operable communication with the plurality of video processing pipelines.

8. (Previously Presented) The method of claim 7, wherein the number of video decoders is greater than the number of video processing pipelines.

9. (Previously Presented) The method of claim 7, further comprising storing the processed decoded portion of the video data into a portion of a video buffer that is not updating the display.

10. (Previously Presented) The method of claim 9, further comprising switching the portion of the video buffer that is not updating the display with a portion of the video buffer that is updating the display, upon determining that the plurality of video processing pipelines has completed processing the decoded portion of the video data.

11. (Previously Presented) The method of claim 7, wherein decoding, with the plurality of video decoders, the portion of video data comprises decoding, with the plurality of video decoders, a frame in the video data.

12. (Previously Presented) The method of claim 7, wherein decoding, with the plurality of video decoders, the portion of video data comprises decoding, with the plurality of video decoders, a field of a frame in the video data.

13. (Previously Presented) The method of claim 7, wherein decoding, with the plurality of video decoders, the portion of video data comprises decoding, with the plurality of video decoders, a scaled field of a frame in the video data.

14. (Previously Presented) A method for displaying video data from a plurality of video sources via a plurality of video channels in a display device, comprising:

receiving first video data from a first video source at a first video decoder via a first video channel;

receiving second video data from a second video source at a second video decoder via a second video channel;

decoding, via the first video decoder, a first frame of the first video data;

decoding, via the second video decoder, a second frame of the second video data;

inputting the first decoded frame into a first video processing pipeline via a non-blocking switch network;

inputting the second decoded frame into a second video processing pipeline via the non-blocking switch network;

processing, by the first video processing pipeline, the first decoded frame;

processing, by the second video processing pipeline, the second decoded frame;

transmitting the processed first decoded frame into a first portion of a video buffer for updating the display device with the processed first decoded frame;

storing the second processed decoded frame into a second portion of the video buffer that is not updating the display device; and

providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

15. (Previously Presented) The method of claim 14, wherein processing, by first video processing pipeline, the decoded first frame comprises determining whether a first video source coupled to the first video processing pipeline is in a failed state.

16. (Previously Presented) The method of claim 15, wherein processing, by the first video processing pipeline, the first decoded frame comprises outputting a blacked out frame for the first video source upon determining that the first video source is in a failed state.

17. (Previously Presented) The method of claim 14, further comprising switching the configuration of the second portion of the video buffer that is not updating the display with the configuration of the first portion of the video buffer that is updating the display upon determining that the first and second video processing pipelines have completed processing the first and second decoded frames.

18. (Previously Presented) The method of claim 14, wherein performing the following for each of the plurality of video sources further comprises scaling the first and second decoded frames based on the image size and the number of video sources.

19. (Previously Presented) A system for displaying video data on a display device comprising:

a plurality of video sources;

a plurality of video channels coupled to the plurality of video sources, wherein each of the plurality of video sources is configured to transmit first video data to a different one of the plurality of video channels; and

a video logic coupled to the plurality of video channels, the video logic comprising:

a plurality of video decoders, wherein each of the plurality of video decoders is configured to receive the first video data from a different one of the plurality of video sources and to decode the first video data;

a plurality of video processing pipelines; and

a switch network coupled to the plurality of video decoders and the plurality of video processing pipelines, the switch network configured to connect any of the plurality of video decoders to any of the plurality of video processing pipelines, wherein one of the plurality of video processing pipelines is configured to process the decoded first video data from a portion of the plurality of video decoders, and

a manual I/O interface in operable communication with the plurality of video processing pipelines, the manual I/O interface being configured to provide an option to a user to direct the switch network to display the first video data in a particular view window of the display device.

20. (Previously Presented) The system of claim 19, wherein the video logic further comprises an image size/location logic coupled to the plurality of video processing pipelines, the image size/location logic configured to receive a control input for a size and a location of a window in the video display terminal and a designated number of video sources to display in the window, wherein the image size/location logic is further configured to determine a location in the window and a size of a part of the window for display for the first video data for each of the designated video sources.

21. (Previously Presented) The system of claim 20, wherein the video logic further comprises a plurality of scalers coupled to the plurality of video decoders and the plurality of video processing pipelines, wherein each of the plurality of scalers is configured to scale the decoded first video data from one of the video sources based on the size of the part of the window determined by the image size/location logic.

22. (Previously Presented) The system of claim 19, wherein the video logic comprises a greater number of video decoders than video processing pipelines and wherein the video logic further comprises a display/control logic coupled to the plurality of video processing pipelines, the display/control logic configured to control an order of processing of the decoded first video data in the designated video sources by the number of video processing pipelines.

23. (Previously Presented) The system of claim 19, wherein the one of the plurality of video processing pipelines is configured to execute a video fail operation if one of the plurality of video decoders does not lock onto the first video data from one of the plurality of video sources within a predetermined time.

24. (Previously Presented) The system of claim 23, wherein the video fail operation comprises an output of a blacked out frame overlaid with a descriptive text to indicate video failure for the one of the video sources.

25. (Previously Presented) The system of claim 23, wherein the video fail operation comprises an output of a previous image for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure.

26. (Previously Presented) The system of claim 19, wherein the first video data is analog video data.

27. (Previously Presented) The system of claim 19, wherein the video logic further comprises a write multiplexer and a video buffer coupled to the plurality of video processing pipelines, wherein the write multiplexer is configured to write the processed decoded first video data from the plurality of video processing pipelines into the video buffer.

28. (Original) The system of claim 27, wherein the video logic further comprises a clock multiplier network, the clock multiplier network to control a rate of operation of the write multiplexer.

29. (Cancelled).

## XI. Evidence Appendix

No evidence pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 has been entered by the Examiner or relied upon by Appellant in the instant appeal beyond that which is already contained in the as-filed application, as is delineated in the Arguments section of this Brief.

## XII. Related Proceedings Appendix

As there are no related appeals and interferences, there are also no decisions rendered by a court or the Board of Patent Appeals and Interferences that are related to the instant appeal.